## **Will Yelton, WORK LOG**

**MILESTONE 1 WORK:**

Tuesday, January 14, 2020

Met with team [4.5 hours]

* We decided on a very modified load-store design and planned out the whole thing including instructions, transferring it to machine code, and a little bit of discussion about physical architecture and efficiency.
* I worked on writing the code for Euclid’s algorithm and giving a lot of input on the architecture design.

Wednesday, January 15, 2020

Corrected some errors in the Euclid’s Algorithm Code [30 min]

* Changed li to lli
* Added the machine code for J and Jal
* Changed the immediates in the load and store word commands to load/store in the correct place on the stack for our architecture.

Met with team [15 min]

* Decided on Milestone 2 tasks
* Some miscellaneous fixes for the design document and instructions

My tasks for Milestone 2:

1. Work on RTL instructions (all of us will do this)
2. Start working on an assembler

**MILESTONE 2 WORK:**

Tuesday, January 20. 2020

Wrote a basic assembler [30 min]

Corrected some errors in the design document [30 min]

Met with team [2 hours]

* Wrote the RTL for all or our instructions
* Discussed some aspects of the datapath
  + Created some designs for some components (like register file)

Wednesday, January 21, 2020

Added error checking and some more features to the assembler [1 hour]

Met with team [30 min]

* Corrected some errors in the design document
* Finished up some work on Milestone 2 (components for RTL instructions)
* Fixed comments in Euclid’s algorithm code

Tasks for milestone 3:

* Create some hardware components
  + Not decided who is doing which components
* Finalize assembler
  + Make labels work properly
* Work on component tests